STIC Search Report
EIC 2800

STIC Database Tracking Number: 123537

TO: Monica Lewis **Location:** **Art Unit : 2822** **Wednesday, June 09, 2004** **Case Serial Number: 09/993967**	**From: Scott Hertzog** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **Scott.hertzog@uspto.gov**

Search Notes

Examiner Lewis,

Attached are edited search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact:***

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

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File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info

Ref    Items  Index-term
E1         1  CR=JP 01156736, 1987, YOSHIZAWA T
E2         1  CR=JP 01157947, 1989, ARAI K
E3         0 *CR=JP 01158768
E4         1  CR=JP 01159030, 1989, TOKUMITSU S
E5         1  CR=JP 01159906, 1989, TACHIKA H
E6         1  CR=JP 01159908, 1989, ECHIGO S
E7         2  CR=JP 01160995, 1989, YOSHIHAMA M
E8         1  CR=JP 01161066, 1989
E9         1  CR=JP 01161123, 1989, MITO Y
E10        1  CR=JP 01163674, 1990, WHITELEY SR
E11        1  CR=JP 01163802, SHIN S
E12        1  CR=JP 01165582, 1989
Ref    Items  Index-term
E1         1  CR=JP 0114754, 1998, JAPAN ENERGY KK
E2         1  CR=JP 0114757J, 2001, KOIZUMI F
E3         0 *CR=JP 01147860
E4         1  CR=JP 0114798, 1998
E5         1  CR=JP 01149045, 1987, KANEKO Y
E6         1  CR=JP 01149766, 1989, NAKANO Y
E7         1  CR=JP 01149828, WATANABE Y
E8         1  CR=JP 01149846, 1989
E9         1  CR=JP 01152456, 1987, TANAKA S
E10        1  CR=JP 01154701, 1989, TAGAWA K
E11        1  CR=JP 01154702, 1989, FUJIMURA S
E12        1  CR=JP 01154703, 1989, TAGAWA K

Set      Items   Description
S1         267   CA='EMA T'
S2       29758   STI OR TRENCH? OR GROOVE? OR ULSI OR VERTICAL(2N)(DRAM OR -
                 CAPACIT? OR TRANSISTOR? OR MEMOR?)
S3           7   S1 AND S2
S4          11   CA='EMA Y'
S5           0   S2 AND S4
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     FILE 'DPCI' ENTERED AT 15:26:26 ON 08 JUN 2004
L1             1 S US 2002076880/PN
L2               SEL L1 1- PN.D :       3 TERMS
L3            10 S L2
L4               SEL L3 1- PN.G :     117 TERMS
L5           810 S L4
L6               SEL L5 1- PN.G :   11081 TERMS
L7               SEL L5 1- PRN :    1210 TERMS
L8         53749 S L6
L9               SEL L8 1-10000 PRN :     827 TERMS  (SELECT ENDED BY USER)

     FILE 'HCAPLUS, WPIX' ENTERED AT 15:41:28 ON 08 JUN 2004
L10         1646 S L7
L11         1477 S L9
L12       435877 S STI OR TRENCH? OR GROOVE? OR ULSI OR VERTICAL(2N)(DRAM OR
                 CAPACITOR? OR TRANSISTOR? OR MEMOR?)
L13          753 S L10 AND L12
L14      3574238 S BOTTOM# OR LOWER# OR UPPER# OR TOP# OR UNDERSIDE# OR
                 UNDER(W) SIDE#
L15          346 S L13 AND L14
L16          296 DUP REM L15 (50 DUPLICATES REMOVED)
L17           94 S L16 AND (BOTTLE? OR COLLAR? OR BURYING OR BURIE#)
L18         4319 S VERTICAL(2N)(DRAM OR CAPACITOR? OR TRANSISTOR? OR MEMOR?)
L19           19 S L17 AND L18
L20           19 DUP REM L19 (0 DUPLICATES REMOVED)
```

File 2:**INSPEC 1969-2004/**May W5
(c) 2004 Institution of Electrical Engineers
File 6:**NTIS 1964-2004/**Jun W1
(c) 2004 NTIS, Intl Cpyrght All Rights Res
File 8:**Ei Compendex(R) 1970-2004/**May W5
(c) 2004 Elsevier Eng. Info. Inc.
File 25:**Weldasearch 19662004/**Dec
(c) 2004 TWI Ltd
File 34:**SciSearch(R) Cited Ref Sci 1990-2004/**May W5
(c) 2004 Inst for Sci Info
File 434:**SciSearch(R) Cited Ref Sci 1974-1989/**Dec
(c) 1998 Inst for Sci Info
File 35:**Dissertation Abs Online 1861-2004/**May
(c) 2004 ProQuest Info&Learning
File 65:**Inside Conferences 1993-2004/**Jun W1
(c) 2004 BLDSC all rts. reserv.
File 94:**JICST-EPlus 1985-2004/**May W3
(c)2004 Japan Science and Tech Corp(JST)
File 99:**Wilson Appl. Sci & Tech Abs 1983-2004/**May
(c) 2004 The HW Wilson Co.
File 103:**Energy SciTec 1974-2004/**May B2
(c) 2004 Contains copyrighted material
File 144:**Pascal 1973-2004/**May W5
(c) 2004 INIST/CNRS
File 239:**Mathsci 1940-2004/**Jul
(c) 2004 American Mathematical Society
File 241:**Elec. Power DB** 1972-1999Jan
(c) 1999 Electric Power Research Inst.Inc
File 305:**Analytical Abstracts 1980-2004/**May W3
(c) 2004 Royal Soc Chemistry
File 315:**ChemEng & Biotec Abs 1970-2004/**May
(c) 2004 DECHEMA
File 987:**TULSA (Petroleum Abs) 1965-2004/**Jun W2
(c)2004 The University of Tulsa

Set	Items	Description
S1	145480	STI OR TRENCH? OR GROOVE? OR ULSI OR VERTICAL(2N)(DRAM OR CAPACITOR? OR TRANSISTOR? OR MEMOR?)
S2	3407799	BOTTOM? ? OR LOWER? ? OR UPPER? ? OR TOP? ? OR UNDERSIDE? ? OR UNDER(W)SIDE? ?
S3	126329	TRENCH? OR GROOVE?
S4	2488803	MEMORY? OR MEMORIE? RAM? OR DRAM? OR RDRAM? OR SDRAM? OR STOR???? OR REGISTER?
S5	25345	COLL?R?
S6	13	S1 AND S2 AND S4 AND S5
S7	10	RD (unique items)
S8	**8**	**S7 NOT PY>2000**
S9	628541	MEMORIE? OR RAM?
S10	2	S1 AND S2 AND S9 AND S5
S11	2	S10 NOT S6
S12	2	RD (unique items)
S13	1	S12 NOT PY>2000
S14	1569181	CAPACIT? OR (STOR???? OR CONDENS?)(2N)(CHARG? OR ELECTRIC? OR ELECTRONIC? OR ELECTRIC? OR ENERG????? OR Q) OR DIELECTR?(-2N)DEVICE? OR VARACT? OR ELECTRET? OR CC=B2130 OR DE=Q-FACTOR
S15	3040369	MEMORY? OR MEMORIE? OR RAM? OR DRAM? OR RDRAM? OR SDRAM? OR STOR???? OR REGISTER?
S16	24	S14 AND S15 AND S3 AND S5
S17	14	S16 NOT PY>2000 NOT S12 NOT S6
S18	**8**	**RD (unique items)**

Date 6/2/04 Serial # 09/993,967 Priority Application Date 2000/206

Your Name M. Lewis Examiner # 73172

AU 2892 Phone 272-1738 Room 7A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-8 + 21-28

Problem: See page 5 lines 1-21

Solution: " " " 23-27

" 6 " 1-17

+ abstract

Staff Use Only

Searcher HENTZ

Searcher Phone: 2-2663

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 6/7/4

Date Completed: 6/9/4

Searcher Prep/Rev Time: 390

Online Time: 76

Type of Search

Structure (#)_____

Bibliographic ✓

Litigation_____

Fulltext_____

Patent Family_____

Other_____

Vendors

STN ✓

Dialog ✓

Questel/Orbit_____

Lexis-Nexis_____

WWW/Internet_____

Other _____

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 12 7355

Application P.Family

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 429 (E-823), 25 September 1989 (1989-09-25) -& JP 01 158768 A (FUJITSU LTD), 21 June 1989 (1989-06-21) * abstract; figure 2 *	1	H01L21/8242 H01L29/786 H01L27/108
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 407 (E-818), 8 September 1989 (1989-09-08) -& JP 01 147860 A (FUJITSU LTD), 9 June 1989 (1989-06-09) * abstract; figure 2 *	1	
A	RUPP T ET AL: "Extending trench DRAM technology to 0.15 /spl mu/m groundrule and beyond" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA,IEEE, US, 5 December 1999 (1999-12-05), pages 33-36, XP010372011 ISBN: 0-7803-5410-9 * figures 3,5 *	1-20	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
A	"HIGH DENSITY VERTICAL DRAM CELL" IBM TECHNICAL DISCLOSURE BULLETIN, IBM CORP. NEW YORK, US, vol. 29, no. 5, 1 October 1986 (1986-10-01), pages 2335-2340, XP000097350 ISSN: 0018-8689 * the whole document *	1-20	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	6 March 2002	Agne, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

☐ L20 ANSWER 1 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number

2001:137520 HCAPLUS Full Text

Title

Method for fabricating 4F2 memory cells with vertical transistor and stacked capacitor

Author/Inventor

Park, Young-Jin; Lee, Heon

Patent Assignee/Corporate Source

Infineon Technologies North America Corp., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 2001013429	A1	20010222	WO 2000-US20554	20000728 <--
US 6355520	B1	20020312	US 1999-374537	19990816
TW 456032	B	20010921	TW 2000-89116436	20000824 <--

Abstract

In accordance with the present invention, a method for forming gate conductors in 4F2 area stacked capacitor memory cells includes the steps of forming a ***buried*** bit line in a substrate, forming an active area above and in contact with the ***buried*** bit line and separating portions of the active area by forming a dielec. material in ***trenches*** around the portions of the active area. Portions of the dielec. material are removed adjacent to and selective to the portions of the active area. A 1st portion of a gate conductor is formed in locations from which the portion of dielec. material is removed, and a 2nd portion of the gate conductor is formed on a ***top*** surface of the dielec. material and in contact with the 1st portion of the gate conductor. Stacked capacitors are formed such that the gate conductor activates an access transistor formed in the portions of the active area.

Concept or Classification

76-3 (Electric Phenomena)

Supplementary Terms

semiconductor ***memory*** device fabrication ***vertical*** ***transistor*** stacked ***capacitor***

Controlled or Index Terms

Capacitor electrodes
Capacitors
Semiconductor device fabrication
Semiconductor memory devices
Transistors
(method for fabricating 4F2 ***memory*** cells with ***vertical*** ***transistor*** and stacked capacitor)
Silicides
RL: DEV (Device component use); USES (Uses)
(method for fabricating 4F2 ***memory*** cells with ***vertical*** ***transistor*** and stacked capacitor)
7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; method for fabricating 4F2 ***memory*** cells with ***vertical*** ***transistor*** and stacked capacitor)

International Patent Classification
ICM H01L021-8242
ICS H01L027-108

☐ L20 ANSWER 2 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
2000:891600 HCAPLUS Full Text

Title
Trench *-gated vertical combination JFET and MOSFET device* ***fabrication***

Author/Inventor
Liu, Yowjuang W.; Wollesen, Donald L.

Patent Assignee/Corporate Source
Advanced Micro Devices, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6163052	A	20001219	US 1997-991464	19971216 <--
US 5864158	A	19990126	US 1997-832657	19970404

Abstract
A combination vertical MOSFET and JFET device (18,22) is formed in a mesa (20,24) of semiconductor material. A ***top*** gate (44,68) of the device is formed by creating a preferably annular ***trench*** (36,58) that extends downwardly from the surface of the semiconductor layer, creating a thin gate insulator (41,62) on the ***bottom*** and sidewalls of this ***trench*** , and filling the ***trench*** with highly doped polysilicon. A ***buried*** gate region (28,50) is formed by implanting the semiconductor layer, prior to ***top*** gate formation, such that the ***buried*** gate region is laterally coextensive with the mesa. An ***upper*** boundary (29,54) of the ***buried*** gate region is spaced below the ***bottom*** of the ***trench*** and spaced from the semiconductor surface. Upon application of a suitable voltage, the ***buried*** gate region and the ***top*** gate region coact to invert the conductivity type of the channel region, permitting transistor operation between the source region and the drain region.

Concept or Classification
76-3 (Electric Phenomena)

Supplementary Terms
trench gated JFET MOSFET fabrication

Controlled or Index Terms
Field effect ***transistors***
MOSFET (***transistors***)
Semiconductor device fabrication
(***trench*** -gated ***vertical*** combination JFET and MOSFET device fabrication)
Dielectric films
Dielectric films
Dopants
Doping
Ion implantation
Semiconductor films
(***trench*** -gated vertical combination JFET and MOSFET device

fabrication using)
7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(poly; ***trench*** -gated vertical combination JFET and MOSFET device fabrication using)

National Patent Classification
257334000

International Patent Classification
ICM H01L029-76
ICS H01L029-94; H01L031-062; H01L031-113

☐ L20 ANSWER 3 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN

Accession Number
1993:114700 HCAPLUS Full Text

Title
Fabricating an integrated circuit comprising integrated injection logic (I2L) and vertical complementary bipolar transistors

Author/Inventor
Kanda, Akihiro; Tanaka, Mitsuo; Hirai, Takehiro; Nakatani, Masahiro

Patent Assignee/Corporate Source
Matsushita Electric Industrial Co., Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5162252	A	19921110	US 1991-808691	19911217 <--
JP 05063150	A2	19930312	JP 1991-291194	19911107 <--
JP 2524035	B2	19960814		
EP 521219	A2	19930107	EP 1991-311763	19911218 <--
EP 521219	A3	19940831		
(1) EP 521219	B1	19980225		
US 5323054	A	19940621	US 1992-907470	19920701 <--

(1) **R:** DE, FR, GB, NL

Abstract
The I2L comprises an emitter, a base, and a collector which are, resp., an n+-type 1st ***buried*** layer, a p+-type 2nd ***buried*** layer having a ***lower*** impurity concentration than the 1st ***buried*** layer, and ≥1 n+-type diffused layer. This structure makes it possible to increase the emitter injection efficiency while the base impurity concentration is kept high, and also to decrease the base width, so that the collector-emitter breakdown voltage and current gain of the I2L can be further improved and its operating speed can be increased.

Concept or Classification
76-3 (Electric Phenomena)

National Patent Classification
437055000

International Patent Classification
ICM H01L021-70
ICS H01L027-00

☐ L20 ANSWER 4 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

2004-236384 [22] WPIX Full Text

Title

Production of memory array on semiconductor substrate by forming word lines in trenches and extending to channel regions of access transistors on bit lines, and filling the trenches with dielectric material to bury the word lines.

Author/Inventor

AHN, K Y; FORBES, L; NOBLE, W P

Patent Assignee/Corporate Source

(MICR-N) MICRON TECHNOLOGY INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6689660	B1	20040210	(200422)*		23	H01L021-336

Application Details

US 6689660 B1 Div ex US 1997-889463 19970708, US 2000-527981 20000317

Priority Application Information

US 1997-889463 19970708 ; US 2000-527981 20000317

Abstract

US 6689660 B UPAB: 20040331

NOVELTY - Memory array is produced on semiconductor substrate by forming word lines are in each of second ***trenches*** , in which word lines extends to channel regions of access transistors on respective alternate bit line. The second ***trenches*** are filled with a dielectric material to bury the word lines in the second ***trenches***.

DETAILED DESCRIPTION - Production of memory array on semiconductor substrate involves forming semiconducting layers on a substrate surface. The semiconducting layers sequentially include first layer of a first conductivity type, a second layer of a second conductivity type and a third layer of the first conductivity type. First ***trenches*** (220-222) are formed in the semiconducting layers to form bars, each functioning as a bit line (202, 204) for the memory array. Second ***trenches*** are formed in the semiconducting layers in an orthogonal direction to the direction of the bit lines to define in-line access transistors (130) on each of the bit lines. Each access ***transistor*** has a ***vertical*** channel region, defined by the second layer of material and exposed in a sidewall of one of the second ***trenches*** . A gate oxide is formed on the sidewall of the second ***trenches*** , overlying the channel regions of alternating access transistors on first alternate bit lines and overlying the channel regions of alternate access transistors on the bit lines. First and second word lines (206-208) are formed in each of the second ***trenches*** , in which the first word line extends to the channel regions of the access transistors on first alternate bit lines and the second word line extends to the channel regions of the access transistors on the second alternate bit lines. The second ***trenches*** are filled with a dielectric material to bury the first and second word lines in the dielectric material in the second ***trenches***.

USE - For producing memory array on semiconductor substrate (claimed) useful for semiconductor memory devices, e.g. dynamic random access memories.

ADVANTAGE - Provides minimized memory cell (112) surface area (preferably approx. 4 F2 in size) while maintaining folded bit line

structure. The memory array has high density, improved topography, and low noise.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of a portion of a semiconductor memory device produced using bulk silicon processing technique and illustrating the memory cells of the device.

Memory cell 112
Access transistors 130
Storage capacitor 132
Bit lines 202, 204
Word lines 206-208
Trenches 220-222 Dwg.2/8

International Patent Classification
ICM H01L021-336
ICS H01L021-8238; H01L021-8242

☐ L20 ANSWER 5 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number
2001-041409 [05] WPIX Full Text

Title
Aligning a strap diffusion to gate conductor edge of vertical transistor for semiconductor memories involves diffusing dopants from dopant rich material into adjacent substrate region to form strap diffusion.

Author/Inventor
GRUENING, U; MANDELMAN, J A; MICHAELIS, A

Patent Assignee/Corporate Source
(INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP; (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES AG; (SIEI) INFINEON TECHNOLOGIES NORTH AMERICA CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) WO 2000077848	A1	20001221	(200105)*	EN	29	H01L021-8242
TW 488036	A	20020521	(200320)			H01L021-8242
US 6555862	B1	20030429	(200331)			H01L027-108

(1) **RW:** AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE **W:** CN JP KR

Application Details
WO 2000077848 A1 WO 2000-US14922 20000531; TW 488036 A TW 2000-111293 20000626; US 6555862 B1 Div ex US 1999-329705 19990610, US 2000-670745 20000927

Priority Application Information
US 1999-329705 19990610 ; US 2000-670745 20000927

Abstract
WO 200077848 A UPAB: 20010124
NOVELTY - Dopant rich material is deposited on ***buried*** strap on ***top*** of storage node formed in ***trench*** in substrate. ***Trench top*** dielectric is formed on material and portions of material above dielectric are removed. Dopants from material are diffused out into adjacent substrate region to form strap diffusion by forming gate in ***trench upper*** portion so strap diffusion is operatively disposed relative to gate.

DETAILED DESCRIPTION - The dopant rich material includes arsenic silicate glass and is deposited with a thickness of 5-20 nm.

Out-diffusing the dopants further includes forming a sacrificial

oxide and a gate dielectric for forming the gate such that the dopants out-diffuse during processing.

The dopant rich material and the ***trench top*** dielectric form a ***top*** surface within the ***trench***. A dielectric cap is formed on the ***trench top*** dielectric and the dopant rich material at the ***top*** surface of the ***trench***.

The ***trench*** can be employed for a ***trench*** capacitor or a ***buried*** bitline.

INDEPENDENT CLAIMS are given for:

(a) a method for aligning a strap diffusion; and

(b) a semiconductor device where a nitride liner is disposed between the dopant rich material and ***trench top*** dielectric for blocking dopants from entering the ***trench top*** dielectric.

USE - Semiconductor memory device production.

ADVANTAGE - Lateral diffusion is decoupled from the diffusion to gate overlap and from the thickness of the ***trench top*** oxide.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a completed ***trench*** capacitor memory cell according to the invention.

Trench 102 Storage node 110

Buried strap 112

Dopant rich layer 120

Trench top dielectric 128

Strap diffusion 135

Gate conductor 142

Shallow ***trench*** isolation regions 144 Nitride cap 148

Bitline contact 154

Channel 158

Bitline 160

Dwg.10/13

International Patent Classification

ICM H01L021-8242; H01L027-108

ICS H01L029-76; H01L029-94

☐ L20 ANSWER 6 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

2000-477387 [42] WPIX Full Text

Title

Trench capacitor isolation layer formation control in semiconductor device, e.g. memory, manufacture includes selective oxide deposition on conductive material formed in trench and on liner formed on trench sidewalls.

Author/Inventor

BEITNER, J; GABRIC, Z; GRUENING, U; LEE, G; SPINDLER, O; TOBBEN, D; BEINTNER, J

Patent Assignee/Corporate Source

(INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 1026740	A2	20000809	(200042)*	EN	15	H01L021-8242
JP 2000223668	A	20000811	(200044)		9	H01L027-108
CN 1263358	A	20000816	(200055)			H01L021-76
US 6177698	B1	20010123	(200107)			H01L027-108
US 6184091	B1	20010206	(200109)			H01L021-336

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
KR 2000057850	A	20000925	(200122)			H01L021-31
TW 459385	A	20011011	(200247)			H01L027-108

(1) **R:** AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Application Details

EP 1026740 A2 EP 2000-100631 20000113; JP 2000223668 A JP 2000-22737 20000131; CN 1263358 A CN 2000-101981 20000201; US 6177698 B1 Div ex US 1999-241756 19990201, US 1999-461599 19991215; US 6184091 B1 US 1999-241756 19990201; KR 2000057850 A KR 2000-4828 20000201; TW 459385 A
TW 2000-101620 20000613

Priority Application Information

US 1999-241756 19990201 ; US 1999-461599 19991215

Abstract

EP 1026740 A UPAB: 20020722
NOVELTY - Selective oxide deposition layer is deposited on conductive material formed in a ***trench*** and on liner formed on sidewalls of the ***trench*** above the conductive material. The deposited layer selectively grows at an increased rate on the conductive material than on the liner, and is removed except for a portion in contact with conductive material, to form an isolation layer on the latter in the ***trench*** .

DETAILED DESCRIPTION - Selective oxide deposition layer preferably comprises an ozone-activated TEOS oxide of thickness 10-200 nm, and is deposited by chemical vapor deposition. The deposited layer selectively grows 5 times faster on the conductive material than on the liner.

The conductive material includes polysilicon which is oxidized below the isolation layer.

The liner preferably comprises nitride and is removed from the ***trench*** sidewalls during the process.

INDEPENDENT CLAIMS are given for:

(a) a method for fabricating a ***vertical transistor*** ; and

(b) a semiconductor memory.

USE - ***Vertical transistor*** and semiconductor memory manufacture (claimed).

ADVANTAGE - The ***trench top*** dielectric has controlled thickness and can withstand the processes needed to fabricate a memory device.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of the semiconductor device having a liner formed on ***trench*** sidewalls and a sub-atmospheric layer deposited on the liner and a ***buried*** strap.

Trench 14
Conductive material 24
Sidewall liner 36
Selective oxide deposition layer 40 Dwg.2/14

International Patent Classification

ICM H01L021-31; H01L021-336; H01L021-76; H01L021-8242; H01L027-108
ICS H01L021-316; H01L021-8239; H01L027-10

☐ L20 ANSWER 7 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1998-311556 [27] WPIX Full Text

Title

High density DRAM cell - incorporating vertical transistors and buried digit lines.

Author/Inventor
GONZALEZ, F
Patent Assignee/Corporate Source
(MICR-N) MICRON TECHNOLOGY INC
Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5753947	A	19980519	(199827)*		29	H01L029-76

Application Details
US 5753947 A US 1995-390295 19950120
Priority Application Information
US 1995-390295 19950120
Abstract
US 5753947 A UPAB: 20000913
A semiconductor substrate comprises many parallel digit lines comprising N+ dopant on a silicon substrate and mutually isolated by dielectric-filled ***trenches*** having a P-type channel stop at the ***bottom*** of each ***trench***. Each digit line includes at least one step-shaped sidewall adjacent to the ***trench*** , at least partly coated by a Ti, Ta, Co or W refractory. A silicon epitaxial layer (705) word line is formed on the digit lines and comprises a P- region above the digit lines doped at 1x1015-1x1016cm-3, an N- storage node in the uppermost surface and a P+ region adjacent to the digit line, doped at 1x1020-1x1021 cm-3. An insulator region on the epitaxial layer has an opening to the N- region, there is a reference polysilicon gate region on the insulator and a capacitor on the epitaxial layer comprising a finned polysilicon region on the insulator and N- regions, a dielectric region on this and a second polysilicon region on the dielectric. Also claimed are: (i) a semiconductor structure as above with the word line being perpendicular to the digit lines and a polysilicon gate at each junction of digit line and word line. (ii) an access transistor formed in a substrate as above with the digit line acting as a drain, the word line acting as a channel and the polysilicon gate adjacent to the word line.

USE - The ***vertical transistors*** are used in very high density DRAMs and devices such as programmable resistors.

ADVANTAGE - There is a threefold increase in the number of transistors per unit area, tolerances are increased and a wider variety of capacitor designs is possible.

Dwg.20/20
International Patent Classification
ICM H01L029-76

☐ L20 ANSWER 8 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number
1998-086148 [08] WPIX Full Text
Title
Method of forming trench transistor and inverter structures - with a smaller substrate footprint for denser integration..
Author/Inventor
WITEK, K E
Patent Assignee/Corporate Source
(MOTI) MOTOROLA INC
Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5705409	A	19980106	(199808)*		32	H01L021-265

Application Details

US 5705409 A US 1995-535397 19950928

Priority Application Information

US 1995-535397 19950928

Abstract

US 5705409 A UPAB: 20000522

(I) Method for forming a semiconductor device comprises: (a) providing a substrate including a ***trench*** with an annular shaped sidewall; (b) forming p-doped and n-doped channel region on different first and second portions of the sidewall; and (c) forming a gate electrode adjacent the sidewall to control current flow in both the channel regions. Also claimed is a process (II) in which: (A) adjacent ***buried*** doped regions are formed with first and second conductivity types respectively, with a semiconductor layer formed over the second; (B) the semiconductor region is doped with first conductivity type dopant such that a first portion overlies the second ***buried*** region, and a second portion doped with second conductivity type dopant overlies the first ***buried*** region, the portions being in close proximity with an interface region between them; (C) a ***trench*** is formed through the interface region to expose the semiconductor portions on opposite sidewalls of the ***trench*** and the first ***buried*** region on the ***bottom*** of the ***trench*** ; (D) forming an oxide over the ***trench*** sidewalls and ***bottom*** , then conductive material, and etching it to form a gate sidewall adjacent the sidewall; (E) forming first doped region of second conductivity above the semiconductor first portion, and a second doped region of the first conductivity over the semiconductor first portion such that the gate sidewall spacer controls the current flow through the first portion of the semiconductor adjacent the sidewall of the ***trench*** and the second portion of the substrate adjacent the sidewall of the ***trench***. Further claimed (III) is the method in which a doping barrier layer is formed with an opening which defines first and third exposed portions with a second between them. A ***trench*** is formed in the second portion to form a ***vertical transistor*** and the first portion doped n-type and the second portion p-type.

USE - Fabrication of ***trench*** transistors.

ADVANTAGE - Fabrication of ***vertical trench transistors*** allows for denser integration circuits and memory cells.

Dwg.8/50

International Patent Classification

ICM H01L021-265

☐ L20 ANSWER 9 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1997-340953 [31] WPIX Full Text

Title

Manufacturing vertical epitaxial SOI transistors - comprises forming transistor within trench in composite substrate having buried contact region.

Author/Inventor

KENNEY, D M

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5641694	A	19970624	(199731)*		24	H01L021-205

Application Details

US 5641694 A US 1994-361606 19941222

Priority Application Information

US 1994-361606 19941222

Abstract

US 5641694 A UPAB: 19980617

Manufacturing a ***vertical*** epitaxial SIO ***transistor*** in a composite substrate having a ***buried*** contact comprises: (a) forming a ***trench*** in the substrate from the surface to the ***buried*** contact, the ***trench*** having an ***upper*** and ***lower*** portion of exposed sidewall; (b) fabricating a transistor entirely within the ***trench*** by; (i) forming a ***lower*** node in the ***lower*** portion of the ***trench*** in electrical contact with the ***buried*** contact region; (ii) selectively growing epitaxial material on the ***upper*** portion of sidewall with the epitaxial direction being laterally inward towards the centre of the ***trench*** and forming in part a bulk region of the transistor and electrically connected to the substrate for receiving a back biasing potential from it; (iii) forming an ***upper*** node of the transistor within an ***upper*** end of the epitaxially grown material; (iv) forming a gate electrode in the centre region of the ***upper*** ***trench*** portion such that when it is biased an inversion layer forms in the bulk region near the gate, extending between the two nodes. Step (ii) includes continuing the epitaxial growth such that material overflows the ***trench*** is planed, patterned, and etched to define a centre region opening within the ***upper*** portion of the ***trench*** sized to receive the gate electrode formed in (iv). Also claimed are: (I) a method of forming a uniform epitaxial material on the sidewalls of a ***trench*** as described above; and (II) a method of forming a number of ***vertical*** epitaxial SOI ***transistors*** .

USE - Used in the manufacture of SOI transistors.

ADVANTAGE - The method provides higher density integrated circuits. Dwg.2/25

International Patent Classification

ICM H01L021-205

ICS H01L021-8242

☐ L20 ANSWER 10 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1997-011376 [01] WPIX Full Text

Title

Vertical memory cell EPROM array - using a floating gate memory cell structure that can be fabricated with reduced cell area and channel length..

Author/Inventor

MORI, K

Patent Assignee/Corporate Source

(TEXI) TEXAS INSTR INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5576567	A	19961119	(199701)*		10	H01L029-788

Application Details

US 5576567 A Div ex US 1990-546490 19900628, Cont of US 1991-805345 19911209, Cont of US 1992-996354 19921222, US 1994-200834 19940222

Priority Application Information

US 1990-546490 19900628 ; US 1991-805345 19911209 ; US 1992-996354 19921222 ; US 1994-200834 19940222

Abstract

US 5576567 A UPAB: 19970102

A ***vertical*** ***memory*** cell array, using vertical floating gate FET memory cells, formed in a substrate of a first conductivity type comprises: multiple rows of ***buried*** drain bitlines of a second conductivity type and a certain width formed in the substrate to form a continuous conductive path along each row; multiple rows of ***buried*** source groundlines of a second conductivity type, each formed substantially under a respective drain bitline to form a continuous conductive path along each row; each drain bitline and source groundline being separated to define a channel layer with a selected channel length of one doping density to form a continuous conductive path along each row; for each row, multiple ***trench*** areas of a selected configuration formed in the substrate, each ***trench*** having substantially vertical sidewalls and a substantially horizontal ***bottom*** , the sidewalls and the ***bottom*** being contiguous and defining an opening down into the substrate of a width less than the certain width of the drain line and extending through the drain line and channel bitline regions and at least partially into the source bitline region, thereby defining corresponding drain and channel regions in the sidewalls of each ***trench*** and source regions at least in the ***bottom*** of each ***trench*** ; for each ***trench*** , a floating gate conductor insulatively disposed vertically into the opening of the ***trench*** , and therefore over the associated channel region, such that the vertical floating gate is capacitively coupled to the channel region in 4 sidewalls of the ***trench*** , each floating gate conductor forming an upwardly opening cavity having a horizontal ***bottom*** surface, each floating gate conductor having 4 substantially vertical sidewalls contiguous with each of substantially horizontal ***bottom*** walls; multiple columns of program gate wordline conductors insulatively disposed over respective columns of ***trenches*** and extending down into the cavities, and therefore over respective floating gates including the horizontal ***bottom*** walls of the floating gates.

USE - Fabrication of an EPROM array of ***vertical*** floating gate ***memory*** cells.

ADVANTAGE - Reduced cell area and channel length; the array can be made contactless; conventional fabrication techniques employed without the need to use sub-micron fabrication technologies. Dwg.1,1a/4

International Patent Classification

ICM H01L029-788

☐ L20 ANSWER 11 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1995-219028 [29] WPIX Full Text

Title

Structure of semiconductor DRAM memory - has vertical metal oxide semiconductor transistor by setting up source and drain domain on either sides of channel, and trench

capacitor.

Author/Inventor

OZAKI, T

Patent Assignee/Corporate Source

(TOKE) TOSHIBA KK

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
JP 07130871	A	19950519	(199529)*		8	H01L021-8242
US 5519236	A	19960521	(199626)		20	H01L027-108

Application Details

JP 07130871 A JP 1993-156453 19930628; US 5519236 A US 1994-266389 19940627

Priority Application Information

JP 1993-156453 19930628

Abstract

JP 07130871 A UPAB: 19950727

The structure has a ***trench*** (12) formed by the regular arrangement of the DRAM cells on a silicon substrate (10). A capacitor is formed by laying an electrode (14) in the ***trench***. A pillar (20) made up of silicon which adjoins the ***trench*** perpendicularly acts as the channel. A source domain (18) and a drain domain (24) set up on either sides of the channel constitute the vertical metal oxide semiconductor transistor of the semiconductor memory unit.

ADVANTAGE - Improves reliability of semiconductor memory. Does not require alignment substrate for manufacturing process. Reduces aspect ratio of pillar without reducing capacitance. Dwg.9/13

International Patent Classification

ICM H01L021-8242; H01L027-108

ICS H01L027-108

☐ L20 ANSWER 12 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1995-338851 [44] WPIX Full Text

Title

Embedded bit line and cylindrical gate assembly. - has bit line formed on semiconductor substrate with vertical transistor assembly superimposed sequentially.

Author/Inventor

HYOUNG-SUB, K; KIM, H

Patent Assignee/Corporate Source

(SMSU) SAMSUNG ELECTRONICS CO LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
FR 2717950	A1	19950929	(199544)*		57	H01L029-792
GB 2288276	A	19951011	(199544)		54	H01L027-108
US 5460994	A	19951024	(199548)		30	H01L021-70
DE 4418352	A1	19951116	(199551)		32	H01L027-108
JP 07273221	A	19951020	(199551)		18	H01L021-8242
US 5547889	A	19960820	(199639)		29	H01L021-70
US 5574299	A	19961112	(199651)		29	H01L027-108
IT 1269825	B	19970415	(199744)			H01L000-00
GB 2288276	B	19980429	(199819)			H01L027-108
KR 9616773	B1	19961220	(199931)			H01L021-82

Application Details

FR 2717950 A1 FR 1994-6390 19940526; GB 2288276 A GB 1994-10762 19940527;
US 5460994 A US 1994-246227 19940518; DE 4418352 A1 DE 1994-4418352 19940526; JP 07273221 A JP 1994-112985 19940526; US 5547889 A Div ex US 1994-246227 19940518, US 1995-442713 19950508; US 5574299 A Div ex US 1994-246227 19940518, US 1995-442712 19950629; IT 1269825 B IT 1994-MI1047
19940524; GB 2288276 B GB 1994-10762 19940527; KR 9616773 B1 KR 1994-6232
19940328

Priority Application Information

KR 1994-6232 19940328

Abstract

FR 2717950 A UPAB: 19951109
The assembly is a single unit in a high density integrated circuit. A bit line (18) is formed on a semiconductor substrate (10). A column of silicon is formed on the bit line with regions acting as drain (23), channel (24) and source (25) formed sequentially. An insulating layer for the gate (26) and the gate line (28) are formed sequentially around the column of silicon. A protective layer (30) separates adjacent gate lines. An insulating layer with a contact opening is formed over the gate lines (28). A capacitance memory cell (46) is formed with a contact to the transistor source region (25).

The assembly forms an embedded bit line with a vertically integrated bit memory cell.

USE/ADVANTAGE - Fabrication of integrated circuit memory with maximum utilisation of active surface area. Dwg.10/26

International Patent Classification

ICM H01L000-00; H01L021-70; H01L021-82; H01L021-8242; H01L029-792
ICS H01L021-76; H01L021-824; H01L023-535; H01L027-00; H01L029-78 H01L027-108

☐ L20 ANSWER 13 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1994-254635 [31] WPIX Full Text

Title

Semiconductor device with monolithic integrated injection logic and vertical bipolar transistors - has IIL P+ base region formed with high density buried collector layer of vertical PNP transistor , and has N+ diffused layer for IIL collector and vertical NPN transistor collector wall, in contact with IIL buried base.

Author/Inventor

HIRAI, T; KANDA, A; NAKATANI, M; TANAKA, M

Patent Assignee/Corporate Source

(MATU) MATSUSHITA ELEC IND CO LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5331198	A	19940719	(199431)*		23	H01L029-730

Application Details

US 5331198 A Div ex US 1991-808691 19911217, US 1992-924986 19920805

Priority Application Information
JP 1991-159268 19910701

Abstract

US 5331198 A UPAB: 19940921

The integrated circuit includes vertical NPN and PNP transistors on the same wafer as integrated injection logic. The IIL structure includes a ***buried*** n+ emitter layer (5) formed in an opposite conductivity substrate, with a ***buried*** base (8) p+ layer formed in the emitter layer and of the same conductivity as the substrate. The base has a ***lower*** impurity density than the emitter. Both ***buried*** layers are contacted by an epitaxial n- semiconductor layer (9) on the substrate, of opposite conductivity to the substrate. A diffused base layer (12), in the ***top*** layer, contacts the ***buried*** base.

A diffused collector n+ layer (31), in a single region or in multiple regions, is a formed in the diffused base and also contacts the ***buried*** base. The base impurity density adjacent the collector is ***lower*** than the emitter impurity density and the decreases monotonically from the emitter toward the collector.

ADVANTAGE - Increased emitter injection efficiency with high base impurity density and reduced base width, for improved collector-emitter breakdown voltage and current gain; increased IIL operating speed; maintains ***vertical*** PNP ***transistor*** Early voltage as collector impurity density not increased. Dwg.3A/12

International Patent Classification

ICM H01L029-730
ICS H01L029-120; H01L029-460

☐ L20 ANSWER 14 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1993-291680 [37] WPIX Full Text

Title

Mfr. of DRAM device with vertical transistor - by forming bit line buried in silicon substrate and word line vertically on surface via trench process and forming charge storage electrode on trench as stacked structure.

Author/Inventor

CHOI, C G; KIM, J S; YOON, H

Patent Assignee/Corporate Source

(HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYUN-N) HYUNDAI ELECTRONICS CO LTD; (HYUN-N) HYUNDAI ELECTRONICS IND INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
JP 05206405	A	19930813	(199337)*		7	H01L027-108
US 5376575	A	19941227	(199506)B		11	H01L021-70
KR 9406679	B1	19940725	(199619)			H01L027-108
US 5504357	A	19960402	(199619)		10	H01L027-108

Application Details

JP 05206405 A JP 1992-256409 19920925; US 5376575 A US 1992-951174 19920924; KR 9406679 B1 KR 1991-16756 19910926; US 5504357 A Div ex US 1992-951174 19920924, US 1994-269218 19940630

Priority Application Information

KR 1991-16756 19910926

Abstract

US 5376575 A UPAB: 19950214 ABEQ treated as Basic Method comprises: etching a first ***trench*** in an Si substrate (1); adding sidewall insulation; etching a second ***trench*** in the ***bottom*** of the first; implanting a bitline junction region (2) in the second ***trench*** ; filling the ***trenches*** with bitline conductor and etching back to form a bitline (3) in the second ***trench*** ; adding oxide over the bitline; etching a slot in the exposed oxide (4') and Si substrate using a wordline mask extending from one sidewall of the first ***trench*** ; forming gate oxide (14) on the exposed sidewall of the first ***trench*** and the slot; depositing wordline conductor and etching back to form a wordline (5) of desired thickness; adding insulation (7) and pad polySi; ion implanting a charge storage electrode junction (8); adding overall oxide; mask etching to form a charge storage electrode contact; and forming an electrode (11) on the contact.

ADVANTAGE - ***Buried*** bit line reduces surface area and the gate can be elongated vertically thus reducing short channel effect so that a high degree of integration can be achieved. Dwg.3/3

JP 05206405 A UPAB: 19960417

23

Dwg.2/9

Dwg.2/9

International Patent Classification

ICM H01L021-70; H01L027-108

☐ L20 ANSWER 15 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1992-032681 [04] WPIX Full Text

Title

Simultaneous formation of trench contact and vertical transistor gate - useful in BICMOS and gives good contact to buried layer and a compact transistor.

Author/Inventor

EKLUND, R H; HAKEN, R

Patent Assignee/Corporate Source

(TEXI) TEXAS INSTR INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5077228	A	19911231	(199204)*			

Application Details

US 5077228 A US 1989-444508 19891201

Priority Application Information

US 1989-444508 19891201

Abstract

US 5077228 A UPAB: 19931006

A method of forming a contact to a ***buried*** layer and an electrode of a ***vertical transistor*** gate simultaneously comprises forming a ***buried*** layer (16), then a ***trench*** sidewalls and ***bottom*** (66) in the substrate (10) to the ***buried*** layer, forming a second ***trench*** (66) in the substrate, and forming an insulating layer (52,54) on the insulating layer and anisotropically etched to expose insulation in the ***bottom*** of the . first ***trench*** , which is then removed to expose the ***buried*** layer. A conductive layer (64,66) is formed into the ***trenches*** to make contact with the ***buried*** layer and form an electrode in the second ***trench***.

Pref. the substrate is crystalline Si, the ***buried*** layer is an FET

source, and the second ***trench*** pref. extends to the ***buried*** layer. Pref. the electrode controls current between the ***buried*** and a surface doped region and pref. the ***buried*** layer is a collector of a bipolar transistor. Pref. the protective and conductive layers are of the same material, pref. poly-Si. Pref. the insulating layer is silica, pref. formed by thermal oxidation of the substrate.

USE/ADVANTAGE - A method of simultaneously forming a ***trench*** contact and ***vertical transistor*** gate (claimed) is provided which is useful for BiCMOS ICs. A high quality contact between the ***buried*** layer and the surface of the IC is provided and the transistor layout is compact. The method is useful for GaAs as well as Si devices and the electrode may be used for a capacitor as well as an FET. 16/16

International Patent Classification

H01L021-70

☐ L20 ANSWER 16 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1991-352560 [48] WPIX Full Text

Title

Lightly doped drain trench FET for ROM and DRAM cells - self-aligned process has improved reliability, electrical breakdown, short channel effects and adjustable threshold voltage.

Author/Inventor

DHONG, S H; HWANG, W

Patent Assignee/Corporate Source

(IBMC) IBM CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5021355	A	19910604	(199148)*			

Application Details

US 5021355 A US 1990-513711 19900518

Priority Application Information

US 1989-355232 19890522 ; US 1990-513711 19900518

Abstract

US 5021355 A UPAB: 19930928

Preparation of self-aligned, lightly doped drain/source field effect ***trench*** transistor for ROM or DRAM cells comprises implanting dopants to form a retrograde well region (15) in an epitaxial layer (12) on a semiconductor substrate (10), forming oxide isolations (16) on the well and doping between them to give first drain junctions (18). A vertical ***trench*** is etched into the well and dopants implanted into its vertical sides by low-angle oblique ion implantation. Si3N4 masking layers are formed on the sidewalls and self-aligned and lightly doped second drain junction regions (24) formed on the walls above the nitride, then ***buried*** source junction (26) below the ***trench bottom*** formed by low-angle implantation. Oxide is grown on the recessed oxide regions and ***trench bottom*** , the nitride mask removed and thin gate oxide grown on the sidewalls, and the ***trench*** filled with poly-Si, which also covers the filled ***trench*** and recessed oxide to form transfer gate (32) and wordline elements (33).

USE/ADVANTAGE - Transistor is useful for ROM and DRAM cells and

has improved electrical breakdown, short-channel effects, and reliability. The threshold voltage of the ***vertical transistor*** may be adjusted by oblique angle ion implantation or ER doping. @(14pp Dwg.No.1/15)@

International Patent Classification

H01L021-26

☐ L20 ANSWER 17 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1989-371944 [51] WPIX Full Text

Title

Integrated self-aligned trench transistor structure - includes trench cmos devices with filled trench gate elements formed on top of buried source junctions.

Author/Inventor

DAVARI, B; HWANG, W; LU, N C

Patent Assignee/Corporate Source

(IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 346632	A	19891220	(198951)*	EN	30	
US 4881105	A	19891114	(199004)		27	
JP 02026063	A	19900129	(199010)			
(2) EP 346632	B1	19960103	(199606)	EN	42	H01L027-08
DE 68925308	E	19960215	(199612)			H01L027-08

(1) **R:** DE FR GB

(2) **R:** DE FR GB

Application Details

EP 346632 A EP 1989-108839 19890517; US 4881105 A US 1988-206148 19880613;
JP 02026063 A JP 1989-93258 19890414; EP 346632 B1 EP 1989-108839 19890517; DE 68925308 E DE 1989-625308 19890517, EP 1989-108839 19890517

Priority Application Information

US 1988-206148 19880613

Abstract

EP 346632 A UPAB: 19930923

Structure comprises: well region (14) formed in epitaxial layer (12); first and second source regions (18,16) formed adjacent each other in the well; conductive ***trenches*** (20,22) forming a gate in each respective source region; a surface drain region (28,30) formed around each filled ***trench*** , forming respective vertical p-channel PMOS and n-channel NMOS ***trench*** transistors; and a conductive region (34) connecting the gate of each ***trench***.

Pref. an oxide isolation layer (38) is provided over epitaxial layer (12) having conductive openings with nitride spacers (36) over the ***trenches***.

USE/ADVANTAGE - In high density VLSI applications; in an embodiment, the structure is provided as a vertical NOR/NAND gate with ***vertical*** strapping ***transistors***. Device having superior performance, packing density and flat topography can be formed by a simple process. 1/23

International Patent Classification

H01L021-82; H01L027-08; H01L029-78

ICM H01L027-08
ICS H01L021-82; H01L029-78

☐ L20 ANSWER 18 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number
1989-146366 [20] WPIX Full Text

Title
DRAM semiconductor memory cell - is formed on insulating layer having buried semiconductor pillar structure formed using trench in silicon layers of SOI.

Author/Inventor
GOTOU, H

Patent Assignee/Corporate Source
(FUIT) FUJITSU LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 315803	A	19890517	(198920)*	EN	14	
JP 01125858	A	19890518	(198926)			
US 5001526	A	19910319	(199114)			
(2) EP 315803	B1	19940105	(199402)	EN	20	H01L027-10
DE 3886899	G	19940217	(199408)			H01L027-10

(1) **R:** DE FR GB
(2) **R:** DE FR GB

Application Details
EP 315803 A EP 1988-117363 19881019; JP 01125858 A JP 1987-283839 19871110; US 5001526 A US 1988-268185 19881107; EP 315803 B1 EP 1988-117363 19881019; DE 3886899 G DE 1988-3886899 19881019, EP 1988-117363 19881019

Priority Application Information
JP 1987-283839 19871110

Abstract
EP 315803 A UPAB: 19930923
A transistor and a capacitor are formed three-dimensionally in an SOI structure. The substrate having the SOI structure is fabricated by bonding two silicon substrates sandwiching a silicon oxide layer. Pillars of silicon layers arranged in a matrix array are formed in the SOI structure by forming a ***trench*** in the silicon layers of the SOI. The ***lower*** portion of the pillar is used as a storage electrode of the capacitor and the ***upper*** portion as active regions of the ***vertical transistor***. In the ***trench*** , doped polysilicon is filled in a ***lower*** portion and functions as a cell plate of the capacitor, so that a dielectric film being formed on the pillar surface.

A gate insulating film and a gate electrode are formed on the ***upper*** side surface of the pillar. The gate electrode is formed self-aligned, connected in the Y-direction but separated in the X-direction, and functions as a word line. A connecting line of the ***upper*** active region of the transistor functions as a bit line.

ADVANTAGE - Only two mask processes are needed and isolation between adjacent cells is excellent in spite of small cell area. 3b/17

International Patent Classification
H01L021-84; H01L027-10; H01L029-68
ICM H01L027-10
ICS H01L021-82; H01L021-84; H01L027-12; H01L029-68

☐ L20 ANSWER 19 OF 19 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN

Accession Number

1989-040399 [06] WPIX Full Text

Title

Memory cell having vertical trench transistor and trench capacitor - mfd. by self-alignment epitaxial growth, giving small word line loading and reduced word line-to-bit coupling capacitance.

Author/Inventor

HWANG, W; LU, C; LU, C C N; LU, C N

Patent Assignee/Corporate Source

(IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 302204	A	19890208	(198906)*	EN	13	
BR 8803628	A	19890214	(198912)			
JP 01045160	A	19890217	(198913)			
AU 8820336	A	19890209	(198914)			
US 4833516	A	19890523	(198924)		11	
CA 1289266	C	19910917	(199145)			
(2) EP 302204	B1	19931027	(199343)	EN	15	H01L021-82
DE 3885185	G	19931202	(199349)			H01L021-82

Application Details

EP 302204 A EP 1988-109622 19880616; JP 01045160 A JP 1988-161082 19880630; US 4833516 A US 1987-81270 19870803; EP 302204 B1 EP 1988-109622 19880616; DE 3885185 G DE 1988-3885185 19880616, EP 1988-109622 19880616

Priority Application Information

US 1987-81270 19870803

Abstract

EP 302204 A UPAB: 19930923

A semiconductor ***vertical transistor*** /storage ***capacitor*** memory cell structure comprises (1) a layer (12,42,44) of epitaxial semiconductor material disposed on a semiconductor substrate (10), (2) a deep ***trench*** storage capacitor structure (16) including an insulative layer (38) on the ***trench*** walls and a polysilicon filling (28) to form a storage capacitor, (3) A shallow Y-shaped ***trench*** (100) access transistor (14) located over the deep ***trench*** (16), the shallow ***trench*** having sidewalls containing an insulation layer (18) and being filled with polysilicon (58); the Y-shaped ***trench*** has horizontal, vertical and tilted sidewalls and (4) a source region (24) dispersed between shallow ***trench*** (100) and deep ***trench*** (10), and drain regions (20,21) disposed in epitaxial layer (12, 42,44).

USE/ADVANTAGE - For a high density DRAM device. Wordline loading is smaller w.r.t. prior art cells due to the inclusion of a self - alignment epitaxial growth process in the fabrication method. Wordline capacitance and wordline-to-bit coupling capacitance are significantly reduced. 1/12

International Patent Classification

G11C011-34; H01L021-82; H01L027-10; H01L029-78

ICM H01L021-82

ICS G11C011-34; H01L021-205; H01L027-10; H01L027-108; H01L029-78

8/9/1 (Item 1 from file: 2)
DIALOG(R)File **2:INSPEC**

6880860 INSPEC Abstract Number: B2001-05-1265D-017
Title: An orthogonal 6F/sup 2/ **trench**-sidewall vertical device cell for 4 Gb/16 Gb **DRAM**
Author(s): Radens, C.J.; Kudelka, S.; Nesbit, L.; Malik, R.; Dyer, T.; Dubuc, C.; Joseph, T.; Seitz, M.; Clevenger, L.; Arnold, N.; Mandelman, J.; Divakaruni, R.; Casarotto, D.; Lea, D.; Jaiprakash, V.C.; Sim, J.; Faltermeier, J.; Low, K.; Strane, J.; Halle, S.; Ye, Q.; Bukofsky, S.; Gruening, U.; Schloesser, T.; Bronner, G.
Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.349-52
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: **2000** Country of Publication: USA 871 pp.
ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191
Conference Date: **10-13 Dec. 2000** Conference Location: San Francisco, CA, USA
Abstract: This paper describes a novel 6F/sup 2/ **trench**-capacitor **DRAM** with a **trench**-sidewall **vertical**-channel array **transistor** . The cell features a line/space pattern for the active area, single-sided buried-strap node contact, **vertical transistor** channel formed along the **upper** region of the **trench** capacitor, a device active area bounded by the isolation **trench** and capacitor **collar**, and a single bit contact per cell.
(8 Refs)
Subfile: B
Descriptors: cellular arrays; **DRAM** chips; isolation technology; MOS **memory** circuits
Identifiers: **trench**-sidewall vertical device cell; **trench** -capacitor **DRAM**; line/space pattern; single-sided buried-strap node contact; device active area; isolation **trench**; capacitor **collar** ; single bit contact; 4 Gbit; 16 Gbit
Class Codes: B1265D (Memory circuits); B2570F (Other MOS integrated circuits); B2550E (Surface treatment (semiconductor technology))
Numerical Indexing: storage capacity 4.3E+09 bit; storage capacity 1.7E+10 bit
Copyright 2001, IEE

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8/9/2 (Item 2 from file: 2)
DIALOG(R)File **2:INSPEC**

6794766 INSPEC Abstract Number: B2001-02-2550E-034
Title: Polysilicon plug recess etch process for sub-quarter micron devices
Author(s): Kaplita, G.; Ranade, R.; Mathad, G.
Conference Title: Plasma Etching Processes for Sub-Quarter Micron Devices. Proceedings of the International Symposium (Electrochemical Society Proceedings Vol.99-30) p.213-19
Publication Date: **2000** Country of Publication: USA x+378 pp.
ISBN: 1 56677 253 2 Material Identity Number: XX-2000-01352
Conference Date: **17-22 Oct. 1999** Conference Location: Honolulu, HI,
Abstract: Recessing of polysilicon in deep **trench** structures after polysilicon fill is critical in forming the capacitors and connecting them to gate transistors. Process requirements are: recess depth control, high

selectivity to nitride mask and oxide **collar** and flat etch profile at the **bottom**. Process results obtained in two reactors are presented. A low pressure ICP high density plasma reactor is ideally suited for this application. Recess depth control is achieved using an optical interferometric end point system. (1 Refs)

Subfile: B

Descriptors: **DRAM** chips; elemental semiconductors; masks; silicon; sputter etching

Identifiers: sub-quarter micron devices; polysilicon plug recess etch process; deep **trench** structures; polysilicon fill; capacitors; gate transistors; process requirements; recess depth control; high selectivity; nitride mask; oxide **collar**; flat etch profile; low pressure ICP high density plasma reactor; optical interferometric end point system; **DRAM** devices; Si

Class Codes: B2550E (Surface treatment (semiconductor technology)); B2520C (Elemental semiconductors); B2570 (Semiconductor integrated circuits); B1265D (Memory circuits)

Chemical Indexing:
Si int - Si el (Elements - 1)
Si sur - Si el (Elements - 1)

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8/9/3 (Item 1 from file: 8)
DIALOG(R)File **8:Ei Compendex(R)**

04394256 E.I. No: EIP96053159578

Title: Toshiba's new capacitor structure for its 1-gigabit **DRAM memory** cell

Author: Anon

Source: Microelectronics Journal v 27 n 2-3 Mar-Jun 1996. p vi

Publication Year: **1996**

CODEN: MICEB9 ISSN: 0026-2692

Journal Announcement: 9606W5

Abstract: Toshiba Corporation's **ULSI** Research Labs officially presented a new **memory** cell with an innovative **trench** capacitor structure at the recent IEDM meeting in Washington D.C. The cell brings closer **memory** (**DRAM**) with a capacity of 1-gigabit and more, and promises **lower** manufacturing costs than existing **memory** cell technology. (Author abstract)

Descriptors: Random access **storage**; Capacitors; Capacitance; Transistors; Dry etching; Cost effectiveness; Oxides; Fabrication

Identifiers: **Trench** capacitor; **Memory** cell technology; **DRAM**; Bottled shape structure; Electron leakage; Single word line; **Collar** oxide layer

Classification Codes:

722.1 (Data Storage, Equipment & Techniques); 704.1 (Electric Components); 701.1 (Electricity: Basic Concepts & Phenomena); 802.2 (Chemical Reactions); 804.2 (Inorganic Components)

722 (Computer Hardware); 704 (Electric Components & Equipment); 701 (Electricity & Magnetism); 802 (Chemical Apparatus & Plants); 804 (Chemical Products)

72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING); 80 (CHEMICAL ENGINEERING)

18/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:**INSPEC**

7342161 INSPEC Abstract Number: B2002-09-1265D-031
Title: Embedded **trench DRAMs** for sub-0.10 mu m generation by using hemispherical-grain technique and LOCOS **collar** process
Author(s): Saida, S.; Sato, T.; Sato, M.; Kito, M.
Conference Title: Proceedings of ISSM2000. Ninth International Symposium on Semiconductor Manufacturing (IEEE Cat. No.00CH37130) p.177-80
Publisher: Ultra Clean Soc, Tokyo, Japan
Publication Date: **2000** Country of Publication: Japan xvii+449 pp.
ISBN: 0 7803 7392 8 Material Identity Number: XX-2002-00929
Conference Sponsor: UCS; IEEE; EDS; SEMI
Conference Date: **26-28 Sept. 2000** Conference Location: Tokyo, Japan
Abstract: For the future System on Chip era, the embedded **DRAM** is one of the most important devices. Since the variety of the devices must be produced in small number, it is difficult to reduce the investment cost. Therefore, its suppression is the key. In this paper, we propose the **trench capacitor** scaling strategy. We show that the strategy realizes 30fF/cell for the 0.08 mu m **trench** and reduces the cost of ownership (COO) and raw process time (RPT) of the 0.08 mu m **trench** to 80% of 0.18 mu m **trench**, with a little investment of $1.6M. It is achieved by the LOCOS **collar** process and HSG technique and so on. (5 Refs)
Subfile: B
Descriptors: **capacitors**; costing; **DRAM** chips; integrated circuit economics; oxidation
Identifiers: embedded **trench DRAMs**; hemispherical-grain technique; LOCOS **collar** process; System on Chip; embedded **DRAM**; investment cost; **trench capacitor** scaling strategy; cost of ownership; raw process time; HSG technique; 0.10 micron; 0.08 micron; 0.18 micron
Class Codes: B1265D (Memory circuits); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); **B2130** (Capacitors); B0170E (Production facilities and engineering
Numerical Indexing: size 1.0E-07 m; size 8.0E-08 m; size 1.8E-07 m

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18/9/2 (Item 2 from file: 2)
DIALOG(R)File 2:**INSPEC**

6368272 INSPEC Abstract Number: B1999-11-1265D-016
Title: A salicide-bridged **trench capacitor** with a double-sacrificial-Si/sub 3/N/sub 4/-sidewall (DSS) for high-performance logic-embedded **DRAMs**
Author(s): Togo, M.; Nobusawa, H.; Hamada, M.; Yoshida, K.; Tanigawa, T.
Journal: NEC Research and Development vol.40, no.3 p.277-81
Publisher: NEC Creative,
Publication Date: **July 1999** Country of Publication: Japan
CODEN: NECRAU ISSN: 0547-051X
Abstract: We propose a double-sacrificial-Si/sub 3/N/sub 4/-sidewall (DSS) technology to develop a salicide-bridged **trench-capacitor** cell for high-performance logic-embedded **DRAMs** . Both the DSS

technology and the salicide-bridging are fully compatible with high-performance CMOS processes. With these technologies, a **storage** node of a substrate-plate **trench** (SPT) **capacitor** can be connected to a drain node even over a thick oxide **collar** during the silicidation. (4 Refs)

Subfile: B

Descriptors: **capacitors**; CMOS **memory** circuits; **DRAM** chips; isolation technology

Identifiers: salicide-bridged **trench capacitor**; double-sacrificial-sidewall; logic-embedded **DRAMs**; high-performance CMOS processes; **storage** node; substrate-plate **trench** **capacitor**; drain node; oxide **collar**; silicidation; Si/sub 3/N/sub 4

Class Codes: B1265D (Memory circuits); **B2130** (Capacitors); B2570D (CMOS integrated circuits); B2550E (Surface treatment (semiconductor technology

Chemical Indexing:

Si3N4 int - Si3 int - N4 int - Si int - N int - Si3N4 bin - Si3 bin - N4 bin - Si bin - N bin (Elements - 2)

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18/9/3 (Item 3 from file: 2)

DIALOG(R)File 2:**INSPEC**

4735628 INSPEC Abstract Number: B9409-2570D-041, C9409-7410D-147

Title: Retrograde well and epitaxial thickness optimization for shallow- and deep-**trench** **collar** merged isolation and node **trench** SPT **DRAM** cell and CMOS logic technology

Author(s): Voldman, S.; Marceau, M.; Baker, A.; Adler, E.; Geissler, S.; Slinkman, J.; Johnson, J.; Paggi, M.

Publisher: IEEE, New York, NY, USA

Publication Date: **1992** Country of Publication: USA 1022 pp.

ISBN: 0 7803 0817 4

Conference Title: Proceedings of IEEE International Electron Devices Meeting p.811-14

Conference Sponsor: Electron Devices Soc. IEEE

Conference Date: 13-16 Dec. 1992 Conference Location: San Francisco, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: A comprehensive study of design point constraints on n-well and epitaxial design for a CMOS **trench** **DRAM**/SRAM/logic process is presented. Design criteria and guidelines, derived from experimentation and process/device simulation, are based on the following considerations: **trench** **DRAM** **storage** node **capacitance**, **DRAM** leakage mechanisms, retention time, n-well electrical parametrics, pnp bipolar current gain, latchup, and electrostatic discharge (ESD) performance. The methodology is discussed for achieving optimum power, signal, retention time, performance, reliability and ESD performance. (11 Refs)

Subfile: B C

Descriptors: circuit reliability; CMOS integrated circuits; digital simulation; **DRAM** chips; electrostatic discharge; logic arrays; logic CAD; semiconductor process modelling

Identifiers: retrograde well; epitaxial thickness optimization; deep-**trench collar** merged isolation; node **trench** SPT **DRAM** cell; CMOS logic technology; substrate plate **trench**; design point constraints; process/device simulation; **storage** node **capacitance**; leakage mechanisms; retention time; n-well electrical parametrics; pnp bipolar current gain; latchup; electrostatic discharge; reliability; shallow-**trench collar** merged isolation

Class Codes: B2570D (CMOS integrated circuits); B1265D (Memory circuits); B1265B (Logic circuits); B2550 (Semiconductor device technology); B1130B (Computer-aided circuit analysis and design); B5110 (Electrostatics); B0170N (Reliability); C7410D (Electronic engineering); C5320G (Semiconductor storage); C5210B (Computer-aided logic design)

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18/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:**INSPEC**

03854522 INSPEC Abstract Number: B91023596

Title: A high performance 16-Mb **DRAM** technology

Author(s): Bakeman, P.; Bergendahl, A.; Hakey, M.; Horak, D.; Luce, S.; Pierson, B.

Conference Title: 1990 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.90CH2874-6) p.11-12

Publisher: IEEE, New York, NY, USA

Publication Date: **1990** Country of Publication: USA xvii+143 pp.

Conference Date: 4-7 June 1990 Conference Location: Honolulu, HI, USA

Abstract: A high performance 16-Mb **DRAM** technology is presented. The key issues that must be considered to achieve high yield and reduced cost are described. Technology elements include: deep **trench capacitor** node with thick oxide **collar** for improved packing density, variable-size shallow **trench** isolation (STI) for device performance and ease of integration, polysilicon surface strap to connect the **capacitor** node to the transfer device, and smoothed dep/etched phosphosilicate glass (PSG) passivation. The application of the above technology elements in conjunction with the MINT cell structure makes it possible to achieve a **DRAM** cell size of 4.13 mu m/sup 2/, using six 0.5- mu m critical-dimension and 0.2- mu m overlay lithography levels. Up to ten sequential process steps are performed in a single cluster. A 50-ns access time has been demonstrated. (6 Refs)

Subfile: B

Descriptors: **DRAM** chips; integrated circuit technology; MOS integrated circuits; passivation; VLSI

Identifiers: ULSI; DUV lithography; smoothed PSG passivation; 16-Mb **DRAM** technology; key issues; yield; deep **trench capacitor** node; thick oxide **collar**; packing density; variable-size shallow **trench** isolation; ease of integration; polysilicon surface strap; glass; MINT cell structure; **DRAM** cell size; access time; 16 Mbit; 0.5 micron; 50 ns

Class Codes: B1265D (Memory circuits); B2570F (Other MOS integrated circuits); B2550E (Surface treatment and oxide film formation)

Numerical Indexing: storage capacity 1.7E+07 bit; size 5.0E-07 m; time 5.0E-08 s

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18/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:**INSPEC**

02842584 INSPEC Abstract Number: B87017093, C87016567
Title: A 4 Mb **DRAM** with cross-point **trench** transistor cell
Author(s): Shah, A.H.; Wang, C.-P.; Womack, R.H.; Gallia, J.D.; Shichijo, H.; Davis, H.E.; Elahy, M.; Banerjee, S.K.; Pollack, G.P.; Richardson, W.F. ; Borderlon, D.M.; Malhi, S.D.S.; Pilch, C.; Tran, B.; Chatterjee, P.K.
Conference Title: 1986 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.86CH2263-2) p.268-9, 369
Editor(s): Winner, L.
Publisher: Lewis Winner, Coral Gables, FL, USA
Publication Date: **1986** Country of Publication: USA 404 pp.
Conference Sponsor: IEEE; Univ. Pennsylvania
Conference Date: 19-21 Feb. 1986 Conference Location: Anaheim, CA, USA
Abstract: An experimental 4-Mb **DRAM** is described that uses a cross-point 1-T cell and a folded bit-line scheme that realizes a truly cross-point **memory** array. It also serves as a demonstration vehicle for 1- mu m CMOS process technology with double-level metal and deep **trenches**. In the cross-point **trench** transistor cell (TTC), the **charge** is **stored** on the polysilicon plug inside the **trench** and the pass transistor is formed around the **collar** of the **trench**. The substrate forms the supply plate for the **capacitor** . The cell is expected to have improved soft-error rate (SER) over conventional 1-T cells because the **stored charge** is oxide-isolated from the substrate. The maximum array density afforded by this cross-point cell was achieved by the folded bit-line method, termed double-ended adaptive folded bit line. (3 Refs)
Descriptors: cellular arrays; CMOS integrated circuits; integrated **memory** circuits; random-access **storage**
Identifiers: soft error rate improvement; dynamic **RAM**; double ended adaptive type; **DRAM**; **trench** transistor cell; folded bit-line scheme; cross-point **memory** array; CMOS process technology; double-level metal; 4 Mbit; 1 micron
Class Codes: B1265D (Memory circuits); B2570D (CMOS integrated circuits); C5320G (Semiconductor storage)
Numerical Indexing: storage capacity 4.2E+06 bit; size 1.0E-06 m

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18/9/6 (Item 1 from file: 94)
DIALOG(R)File 94:**JICST-EPlus**

04251217 JICST ACCESSION NUMBER: 99A0632251 FILE SEGMENT: JICST-E
A Salicide-Bridged **Trench Capacitor** with a
Double-Sacrificial-Si3N4-Sidewall (DSS) for High-Performance
ogic-Embedded **DRAMs**.
TOGO M (1); NOBUSAWA H (1); HAMADA M (1); YOSHIDA K (1); TANIGAWA T (1)
NEC Res Dev, **1999**, VOL.40,NO.3, PAGE.277-281, FIG.14, REF.4
JOURNAL NUMBER: G0138AAA ISSN NO: 0547-051X CODEN: NECRA
ABSTRACT: We propose a Double-Sacrificial-Si3N4-Sidewall (DSS) technology to develop a Salicide-Bridged **trench-capacitor** cell for high-performance logic-embedded **DRAMs**. Both the DSS technology and the Salicide-Bridging are fully compatible with high-performance CMOS processes. With these technologies, a **storage** node of a Substrate-Plate **Trench** (SPT) **capacitor** can

be connected to a drain node even over a thick oxide **collar** during the silicidation. (author abst.)
DESCRIPTORS: logic circuit; **DRAM**; CMOS structure; semiconductor process; device structure; electrostatic **capacity**; thin film condenser; **memory** element; vapor phase growth
BROADER DESCRIPTORS: circuit; **RAM**; **memory**(computer); equipment; dynamic **memory**; MOS structure; production process(control); process; **capacity**; condenser(**capacitor**); circuit component; parts; functional device; crystal growth
CLASSIFICATION CODE(S): NC03162T

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18/9/7 (Item 1 from file: 144)
DIALOG(R)File 144:**Pascal**

14266755 PASCAL Number: 99-0470776
A salicide-bridged **Trench capacitor** with a Double-Sacrificial-Si SUB 3 N SUB 4 -Sidewall (DSS) for high-performance logic-embedded **DRAMs** : Special Issue on Advanced **Memory** Devices and Technologies
TOGO M; NOBUSAWA H; HAMADA M; YOSHIDA K; TANIGAWA T
ULSI Device Development Laboratory, Japan
Journal: NEC research & development, **1999**, 40 (3) 277-281
ISSN: 0547-051X CODEN: NECRAU Availability: INIST-9584; 354000089959470030
We propose a Double-Sacrificial-Si SUB 3 N SUB 4 -Sidewall (DSS) technology to develop a Salicide-Bridged **trench-capacitor** cell for high-performance logic-embedded **DRAMs**. Both the DSS technology and the Salicide-Bridging are fully compatible with high-performance CMOS processes. With these technologies, a **storage** node of a Substrate-Plate **Trench** (SPT) **capacitor** can be connected to a drain node even over a thick oxide **collar** during the silicidation.
English Descriptors: Integrated circuit; Logic circuit; Dynamical **storage**; Random access **memory**(**RAM**); **Capacitance**; High density; Microelectronic fabrication; Technology

French Descriptors: Circuit integre; Circuit logique; Memoire dynamique; Memoire acces direct; **Capacite** electrique; Densite elevee; Fabrication microelectronique; Technologie; Logic-embedded **DRAM**; Salicide; Substrate-plate **trench capacitor**; Oxide **collar**; Vapor-phase doping

Classification Codes: 001D03F06B

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3/9/4 (Item 4 from file: 34)
DIALOG(R)File 34:**SciSearch**(R) Cited Ref Sci

02299858 Genuine Article#: KR138 Number of References: 12
Title: SPREAD-**VERTICAL-CAPACITOR** CELL (SVC) FOR HIGH-DENSITY DRAMS
Author(s): MATSUO N; NAKATA Y; OGAWA H; YABU T; MATSUMOTO S; SASAGO M; HASHIMOTO K; OKADA S
Corporate Source: MATSUSHITA ELECT IND CO LTD,SEMICOND RES CTR/MORIGUCHI/OSAKA 570/JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, **1993**, V40, N4 (APR), P 750-754
ISSN: 0018-9383
Abstract: An advanced 3-dimensionally (3D) stacked-**capacitor** cell, Spread-**Vertical-capacitor** Cell (SVC), was developed. SVC realized a storage capacitance (C(s)) of 30 fF with a cell area of 1.8 mum2, a capacitor height of 0.37 mum, and an equivalent SiO2 film thickness of 7 nm for oxide-nitride-oxide (ONO). By extrapolating these results to 256-Mb dRAM's, a C(s) of 24 fF is obtained with a cell area of 0.5 mum2, a capacitor height of 0.4 mum, and an equivalent SiO2 thickness of 5 nm, and these values satisfy the specifications for 256-Mb dRAM's. Low capacitor height of SVC enables the fabrication process using the ArF excimer laser lithography. SVC is the most promising cell structure for 64-Mb dRAM's and beyond.
Research Fronts: 91-5215 001 (STACKED CAPACITOR STRUCTURE; 33-NS 64-MB DRAM; MERGED MATCH-LINE TEST ARCHITECTURE)
Cited References:
ARIMA H, 1990, P651, IEDM
EMA T, 1988, P592, IEDM
INOUE S, 1989, P31, IEDM

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3/9/5 (Item 5 from file: 34)
DIALOG(R)File 34:**SciSearch**(R) Cited Ref Sci

p
01291931 Genuine Article#: GL709 Number of References: 9
Title: A 33-NS 64-MB DRAM
Author(s): OOWAKI Y; TSUCHIDA K; WATANABE Y; TAKASHIMA D; OHTA M; NAKANO H; WATANABE S; NITAYAMA A; HORIGUCHI F; OHUCHI K; MASUOKA F
Corporate Source: TOSHIBA CO LTD,ULSI RES CTR,KOMUKAI TOSHIBA 1,SAIWAI
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, **1991**, V26, N11, P1498-1505
Language: ENGLISH Document Type: ARTICLE
Geographic Location: JAPAN
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: A 64-Mb CMOS DRAM measuring 176.4 mm2 has been fabricated using a 0.4-mu-m N-substrate triple-well CMOS, double-poly, double-polycide, double-metal process technology. Novel asymmetrical stacked-**trench** capacitor (AST) cells, 0.9 x 1.7-mu-m2 each, are laid out in a newly developed PMOS centered interdigitated twisted bit-line (PCITBL) scheme, which achieves both low noise and high packing density. A high-speed 64-Mb CMOS DRAM with 33-ns access time is

realized by introducing three new circuit techniques that suppress wiring delays.

Cited References:

AOKI M, 1988, P250, ISSCC DIG TECH PAPER
ARIMOTO K, 1989, P244, ISSCC
EMA T, 1988, P592, IEDM
FUJII S, 1989, P248, ISCC
NAKAGOME Y, 1988, V23, P1120, IEEE J SOLID STATE C
NAKAGOME Y, 1990, P17, JUN S VLSI CIRC DIG
OOWAKI Y, 1991, P114, ISSCC
SUNOUCHI K, 1990, P647, IEDM
YOSHIHARA T, 1988, P238, ISSCC DIG TECH PAPER

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3/9/7 (Item 7 from file: 34)
DIALOG(R)File 34:**SciSearch**(R) Cited Ref Sci

00878430 Genuine Article#: FD044 Number of References: 13
Title: A DIVIDED SHARED BIT-LINE SENSING SCHEME FOR **ULSI** DRAM CORES
Author(s): HIDAKA H; MATSUDA Y; FUJISHIMA K
Corporate Source: MITSUBISHI ELECTR CO,LSI RES & DEV LAB,4-1
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, **1991**, V26, N4, P473-478
Abstract: A new DRAM signal sensing principle, a divided/shared bit-line (DSB) sensing scheme, is proposed. This sensing scheme realizes a folded bit-line sensing operation in a crosspoint-type memory cell array. The DSB scheme offers a high-density DRAM memory core with the common-mode array noise eliminated. A bit-line architecture based on this new sensing principle and its operation are demonstrated.

A divided/pausing bit-line sensing (DIPS) scheme is also proposed, which is an application of this DSB principle to the conventional folded bit-line type memory cell arrangement. The DIPS architecture achieves complete pausing states for alternate bit lines throughout the active period. These alternate pausing bit lines shield the inter-bit-line coupling noise between active bit lines. Here the inter-bit-line coupling noise is eliminated by a slight architectural change to the conventional folded bit-line type memory cell array.

These new memory core design alternatives realize high-density DRAM memory cores suitable for the 64-Mb level and beyond, with the memory array noise reduced significantly.

Cited References:

AOKI M, 1988, P250, ISSCC DIG TECH PAPER
EMA T, 1988, P592, IEDM
HIDAKA H, 1990, P15, DIG S VLSI CIRCUITS